

# **BEAR: A Macrocell Layout System For VLSI Circuits**

**By Wei-Ming Dai**



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Timing-Driven Placement for General Cell approach for macrocell layouts which in BEAR-FP, a macro-cell layout system developed at

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the PLD and FPGA compared to ASIC and Gate Array contribute to a significant portion of the extra cost the user has to bear system debug board and layout

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BEAR-FP Manual ~ introduction Introduction BEAR-FP is a macrocell-based layout system which builds on its predecessor, thle BEAR sys- tem [1]. It uses BEAR s

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and the FPGA design will become the new standard for system design. Within the layout geometry, An I/O macrocell for a programmable logic device:

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"Hierarchical Placement and Floorplanning in BEAR," IEEE Trans Maggie Zhi-Wei Kang , Wayne Wei-Ming Dai, simulation of CMOS VLSI circuits under

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